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Temperature Dependence Of Pixel Multichip Module Operating Performance

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Abstract**-- At Fermilab, a research program to developed a pixel detector for the BTeV experiment has been ongoing for the last several years. The basic building block of the pixel detector is the pixel multichip module. Prototypes have been built and characterization tests have been performed to verify that the pixel module will meet the stringent requirements of the experiment. One of these requirements is that the operating temperature of the detector will be at -5°C, which imposes severe constraints on the pixel multichip module packaging design. This paper presents the results on the temperature dependence of the operating performance of the prototype pixel multichip module.**

I. Introduction

THE BTeV experiment is planned to operate in the Silicon C-Zero interaction region of the Tevatron at Fermilab. The vertex detector for this experiment will be a pixel detector composed of 60 pixel planes (assembled in 30 stations) of approximately 100x100 mm^2 each, assembled perpendicular to the colliding beams and installed as close as 6 millimeters from the colliding beams. Each plane is formed by an arrangement of multichip modules with four different lengths: 35 mm, 44 mm, 53 mm and 70 mm. The modules are assembled from up to 8 pixel readout chips bump bonded to a single sensor. The pixel multichip module packaging is composed of three layers. The pixel readout chips form the bottom layer. The back of the chips is in thermal contact with the station supporting structure, while the other side is flip-chip bump bonded to the silicon pixel sensor. A low mass flex-circuit interconnect is glued on the top of this assembly, and the readout IC pads are wire-bounded to the circuit. Due to its proximity to the beam, the pixel multichip module will be exposed to a significant amount of radiation (up to 3 Mrad per year). In order to keep the silicon sensor in operation for over 5 years, the pixel module must operate at a temperature of -5° to –10°C. The low temperature helps to mitigate the effects of radiation damage on the silicon sensors. Since the pixel module will be built at room temperature (23°C), it will have to undergo a temperature variation of around 30°C for many times during it's operating life. The temperature variation can affect several parts of the multichip module packaging: coefficient of thermal expansion (CTE) mismatches can cause the bump-bonds to break, the flex circuit to break off from the pixel sensor, or change the performance of the readout chip. The results presented in this paper shows that the temperature variation has important effects on the pixel modules performance. The performance of the pixel module is similar to the performance of the bare die at low temperature (-5°C).

In this paper we present the results of tests performed to analyze the effects that temperature variation has on the pixel multichip module performance regarding mechanical characteristics (bump bonds reliability) and electrical characteristics , these tests include the measurement of the noise and threshold dispersion of all the cells in the pixel module.

The subjects in test will be on three single chip pixel modules with sensors and one single pixel chip bare die with no sensor (used in this test as a benchmark).

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II. Setup

There were assembled two different test setup, the first one is showed on Fig. 1 and uses a HDI (flex circuit) [1] to provide power and connection lines to data transfer to the readout chip and a HV connection to bias the sensor.

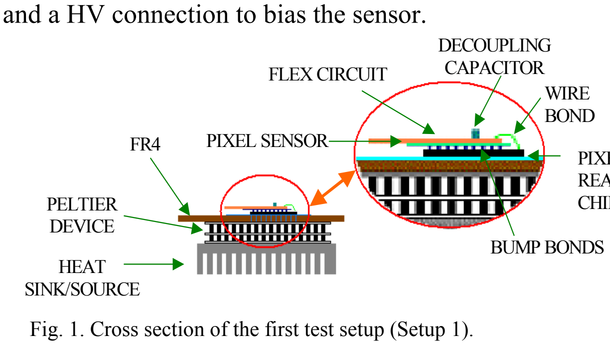

Fig. 1. Cross section of the first test setup (Setup 1).

In this first assembly the HDI is sitting over the sensor that is bump bonded to a readout chip (FPIX 1)[2], the readout chip is wire bonded to the flex circuit. A FR4 board with thermal vias is used to give mechanical support to the assembly and a peltier device is attached to the FR4 board to control the assembly temperature. The sensor has the HV connection glued with conductive epoxy to the HDI.

In Fig. 2 it's possible to observe details of the first setup assembly with the positions of the two RTD (TA,TB) used to measure the temperature indicated in the figure. In the present assembly one readout chip with a sensor bump bonded with indium bumps and a bare die readout chip (FPIX 1) were assembled.

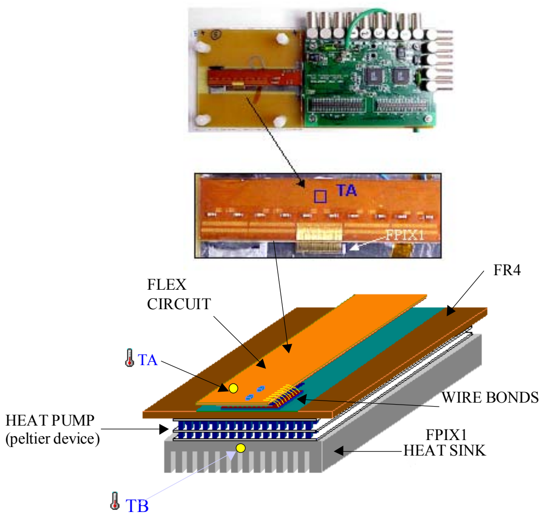

Fig. 2. Assembly details of the first setup, here is possible to observe the readout chip wire bonded to the HDI.

The second test setup was assembled using a PCB to provide power and data connections to the readout chip instead of using a HDI. This setup has two variations, both of them can be observed at Fig. 3 and Fig. 4.

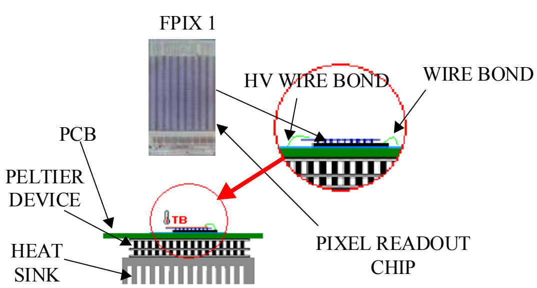

Fig. 3. Cross section of the second test setup (Setup 2A). In the details is possible to observe the readout chip (FPIX 1).

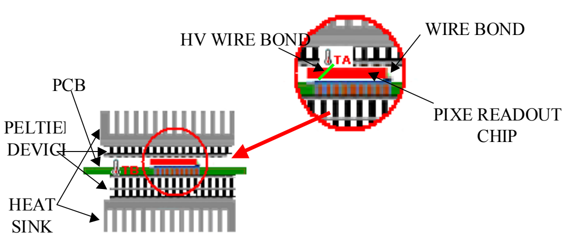

Fig. 4. Cross section of variation of the second setup (Setup 2B). The second Peltier device was used to avoid temperature gradient on the assembly.

This setup is assembled with a PCB to provide mechanical support to the detector and to provide power, a HV connection to the bias the sensor and connection to data transfer from and to the readout chip. In the bottom of the PCB there is a peltier device. The variation in this the setup is showed on Fig. 4 and the only difference between them is the fact that a second peltier device is placed on the top of the detector on the setup 2B. On Fig. 5 a picture of the variation of the second setup is showed.

Fig. 5. Picture of the setup 2B.

III. Bump Bonds Electrical Connectivity Test

Two different kinds of bump bonds were tested, the first one was a Indium bump and the second one the solder bump (Pb/Sn), each one of it using a P-STOP SINTEF sensor bump bonded to a FPIX1 readout chip [3]-[5].

These sensors have around 30 micron pitch, the diameter of the bumps is ~40 microns, and the height is ~15 microns after mating.

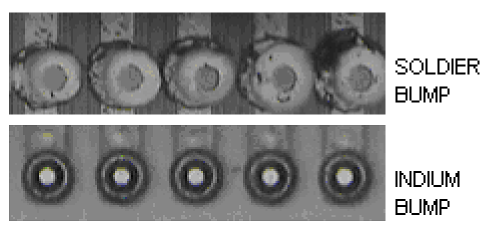

Fig. 6. Picture of the Indium and Soldier bumps.

The first test to be performed was a fast thermo cycle with both ,the Indium bump and the solder bump detectors. This thermo cycle was performed in temperatures range of 5°C to 70°C and it used the Setup 1. The total duration of the this thermo cycle was 120 minutes and it was composed of two steps , the first one took 60 minutes and the temperature was changed from 5°C to 70°C with the temperature raise rate of approximated 1°C per minute. In the second step the temperature was changed from 70°C to 5°C with a fall rate of around 1°C per minute. The humidity during this test was controlled and equal to 15%. In the first test a measurement of the number o cells responding to a injection charge operation was done. The injection charge is characterized by the operation of injecting a charge sufficient to fire each pixel on the readout chip through a special circuit built in the FPIX 1. This operation can simulate real hits on the detector. On Fig. 7 it's possible to observe the behavior of the Indium bump detector regarding the injection charge test.

On Fig. 8 is possible to observe the results of the same test performed for Soldier bump detector.

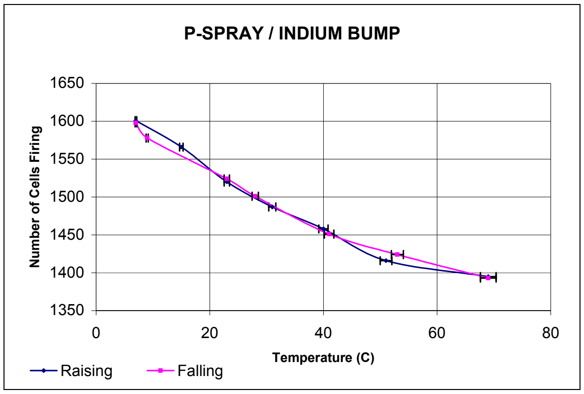

Fig. 7. Number of cells respondig to the injection charge test in the Indium Bump detector.

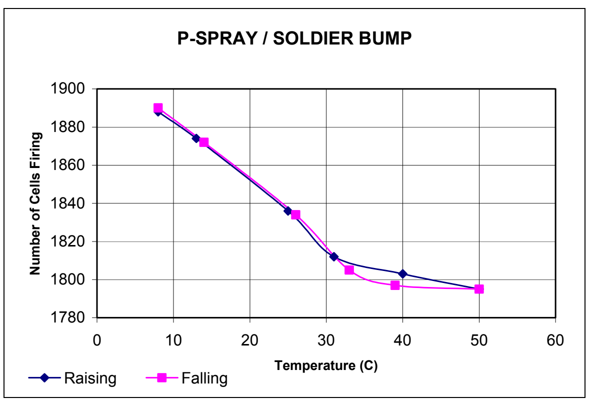

Fig. 8. Number of cells respondig to the injection charge test in the Soldier Bump detector.

The reason why the number of cells firing falls with the increasing of temperature is due to problems with the readout chip and is not related with the sensor or with the bump bonds. This problem is caused by dependence of the temperature of the readout chip (FPIX 1) as can be observed in Fig. 9

Also is possible to be observed that not all the detector is responding but only around 1600 of 2880 cells, this is caused by the same problem in the readout chip, as the temperature goes falling the number of cells responding increases. It's important to observe that the cells that change the status with temperature are located only on the lower edge of the chip, so them can be mapped and exclude for further comparative analysis.

Another factor that should be considered is that there are more cells firing in the soldier bump detector than in the Indium bump detector, this is also related to the problem with the readout chip, these is because each different FPIX 1 respond to a different number of cells, this problem again is restricted to the cells in the lower edge.

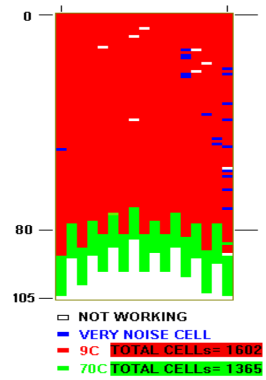

Fig. 9. Injection charge map for two different temperatures, here it's possible to observe the dependece of the temperature dependence of the readout chip.

The important thing to be observed in this test is that we have the same number of cells responding before and after the thermal cycle as can be observed in Fig. 7 and Fig. 8.

The second test performed was a hit map of the detector using a Beta Gun (Sr 90) radiation source. All hit map tests had the duration of 5 minutes. The beta gun was pointed orthogonal to the detector at the distance of 10 cm and directed to the centre of the detector.

On Fig. 10 it's possible to observe the hit map for the soldier bump detector in two different temperatures.

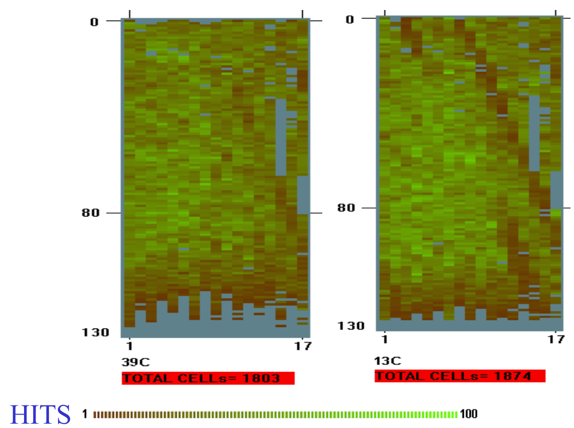

Fig. 10 Hit Map of the Solder bump Detector.

Here there are some cell's that doesn't responded due problems in the bump bonds (gray cells), in the lower edge the cells that are not responding are due reasons that were already explained (readout chip). The reason of the different colors in the cells are due to different number of hits, this is caused by the fact that each cell has a different threshold to fire and also because there are some regions that received more hits than another's.

The resistivity of the bumps can also change the threshold of each cell.

Both detectors were also submitted to a long thermal cycle (LTC) that can be observed in Fig. 11. The long thermal cycle had a total duration of 1080 minutes.

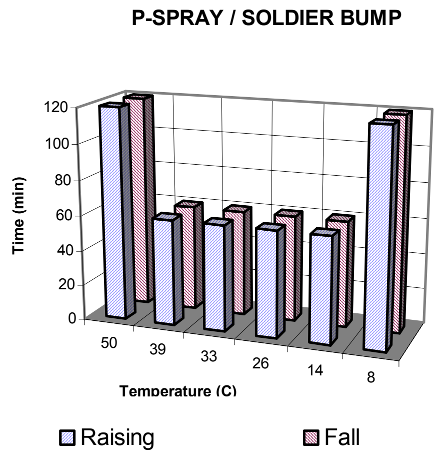

Fig. 11. Characteristics of the long thermo cycle.

The results of the long thermo cycle can be observed at Table I and Table II, it's possible to observe that to avoid the lower edge of the readout chip where the instable cells are, it was analysed in both cases only a region on 900 cells, this region range from column 1 to 15 and from row 1 to 60.

TABLE I- Indium bump Test

Befor LTC	at 7 C	at 42 C
working	868	865
not working	29	29
very noise	3	6
After LTC	at 7 C	at 69 C
working	865	863
not responding	30	29
very noise	5	8

TABLE II- Solder bump Test

Before LTC	at 7 C	at 42 C
working	887	879
not responding	9	9
very noise	4	12
After LTC	at 7 C	at 42 C
working	886	875
not responding	9	9
very noise	5	16

It's possible to observe a slight raise on very noise cells, but the number of working cells doesn't present changes, the difference between them problaby are due to statistical fluctuations. This is possible because as the Beta gun is providing a random pattern of hits on the detector.

IV. Electrical Performance

The following analysis was done to investigate the variation of noise and threshold due temperature variation on the detector.

This test was performed in three diferents devices, the first one was a PSTOP SINTEF detector bump bonded with Indium on a FPIX 1 readout chip, the second one a PSTOP SINTEF detector bump bonded with Soldier bumps on a FPIX 1 readout chip and the third one a bare die readout chip.

The test was performed injectin charge in all cells on the chip this was done using a proper input existing in the readout chip. The pulses injected started at 0.20V and ramping to 1.00V doing a complete scanning in the chip. The threshold of the comparator was setted to 2.00V and the all sensors were biased with –200V.

It is possible to verifie on Fig. 12 that the threshold raises with the temperature and it's similar on all three devices under test. It's important to observe that in the range from 5 to –10 the threshold is constant , it start to raises only after 5 degrees Celsius.

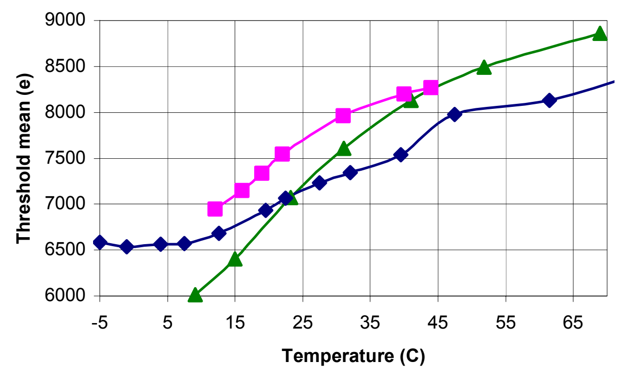

Fig. 12. Threshold mean versus temperature (°C) -Diamond is the bare die chip, triangle is the indium bump detector and square the soldier bump detector.

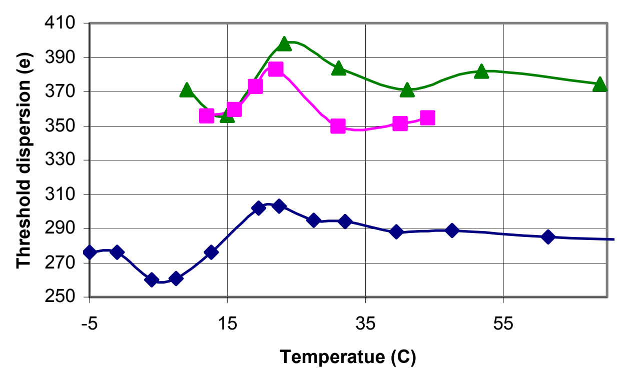

Fig. 13. Threshold dispersion versus temperature (°C) -Diamond is the bare die chip, triangle is the indium bump detector and square the soldier bump detector.

It was also possible to extract the threshold dispersion from the injection scan performed and as it can be observed on Fig. 13 the threshold dispersion for the detectors is around 100 electrons higher than for the bare die. It was verified that for all devices the threshold dispersion raises than fall and stabilize.

The analysis of noise also was possible to be done and in Fig. 14 we can observe that the noise mean behavior it's similar to the threshold dispersion behavior, again the noise mean under 5 degrees is pretty stable and it's possible to observe that the bare die has a noise mean of roughly 100 electrons less than the detectors.

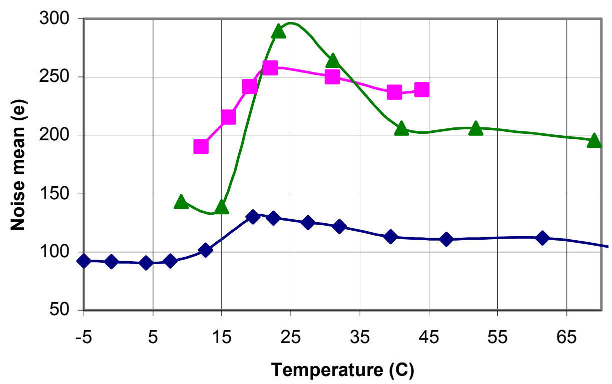

Fig. 14. Noise mean versus temperature (°C) -Diamond is the bare die chip, triangle is the indium bump detector and square the soldier bump detector.

This is due the fact that the bump bond and the sensor increase the noise in the system.

The last analysis that was made was regarding noise dispersion and the results of this analysis can be observed in Fig. 15. The average difference between the noise dispersion in the detectors and in the bare die readout chip is around 20 electrons.

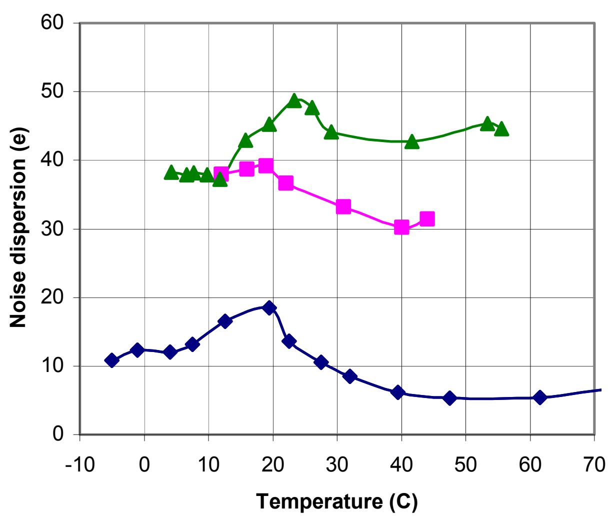

Fig. 15. Noise dispersion versus temperature(°C) -Diamond is the bare die chip, triangle is the indium bump detector and square the soldier bump detector.

V. Conclusions

The results confirm that the performance of the pixel modules and the bare die are equivalent under temperature variations. The differences observed are consistent with the variations found in previous tests with the same readout pixel chip at a constant temperature. This indicates that during the cool down process the packaging performance doesn't degrade due to the stress introduced by CTE mismatches.

No Permanent damage due the thermo cycle was observed in the noise and threshold performance. Both bump bonds had roughly the same noise and threshold performance.

There was no loss in bump bonds during both thermal cycles in all chips tested.

VI. References

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